## ABSTRACT

A memory device having memory cells in which a single access transistor controls the grounding of at least two storage elements, such as resistive storage elements, for purposes of reading the respective logical states of the storage elements. The logical states of the storage elements are decoupled from one another and are read independently. The storage elements are disposed in respective layers. Each storage element is coupled to first and second conductors having respective longitudinal axes. The longitudinal axes are oriented substantially parallel to one another, at least in proximity to a particular storage element.